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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,850	07/10/2003	Sang Hoo Dhong	AUS920020711US1	1815

45327 7590 11/08/2004

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,850	DHONG ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15* is/are rejected.

7)☒ Claim(s) *16-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta et al. (U. S. PAT. 5,821,775) in view of Krishnamurthy et al. (U. S. PAT. 6,204,696).

In claim 1, Mehta et al. teaches all claimed features in Fig. 3A, a method for implementing a logic circuit with integrated logic and latch design, the method comprising the steps of: providing a clock input (170) to the logic circuit; providing one or more (A, B) static signal inputs to the logic circuit; generating one or more dynamic signal inputs (IN1 380, IN1 385) by dynamically gating the one or more static signal inputs with the clock signal; applying the one or more dynamic signal inputs (IN1 380, IN1 385) to the logic circuit; generating one or more dynamic signal outputs (OUT 390) of the logic circuit; precharging (335) the one or more dynamic signal outputs based on the clock signal; evaluating (340) the one or more dynamic signal outputs when the one or more dynamic signal outputs are not being precharged; holding (350) the one or more dynamic signal outputs when the one or more dynamic signal outputs are neither

being precharged nor being evaluated; with the exception of teaching step of converting the one or more dynamic signal outputs into one or more static signal outputs. However, Krishnamurthy et al. teaches in Fig. 1 the conversion of one or more dynamic signal outputs into one or more static signal outputs (14).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Krishnamurthy et al. and the teachings of Mehta et al. to convert an evaluated output signal into a static signal as desired.

In claim 2, Mehta et al. further teaches in Fig. 2A the method of claim 1, wherein the one or more static signal inputs comprise complementary static signal inputs (A#, B#).

In claim 3, Mehta et al. further teaches in Fig. 3A the method of claim 1, wherein the one or more dynamic signal inputs comprise one or more delayed signal inputs (320).

In claim 4, Mehta et al. further teaches in Fig. 3A the method of claim 1 further comprising the step of applying one or more static signal inputs (A, B) to the logic circuit.

In claim 5, Mehta et al. further teaches in Fig. 3A the method of claim 1 wherein the step of evaluating (340) the one or more dynamic signal outputs follows the step of precharging (335) the one or more dynamic signal outputs.

In claim 6, Mehta et al. further teaches in Fig. 3A the method of claim 1 wherein the step of holding (350) the one or more dynamic signal outputs follows the step of evaluating (340) the one or more dynamic signal outputs.

Apparatus claims 7-10 correspond to detailed circuitry already discussed similarly with regard to method claims 1-4.

Apparatus claim 15 corresponds to detailed circuitry already discussed similarly with regard to method claim 1.

3. Claims 16-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER